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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/791,870	OZAWA, YOSHIO	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 06/17/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention I, **claims 1-11 and 20**, in the reply filed on 06/06/2005 is acknowledged.

3. **Claims 12-19** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse, as noted above.

Drawings

4. Figures 7A and 7B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 6 and 9 are objected to because of the following informalities: Claim 9, which depends on claim 6, recites: "the second side-wall insulation film" which lacks an antecedent basis. The one claim that describes a second side-wall insulation film is claim 5. However, claim 9 also recites "the control gate electrode lower layer" whose antecedent basis is provided by claim 6. Therefore, if claim 6 is rewritten to depend on claim 5, claim 9 would have an antecedent basis for "the second side-wall insulation film". Such dependency (1/5/6/9) is interpreted for examination. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4-5, 10, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. U.S. Patent 6,441,429 (the '429 reference) in view of Zheng et al. U.S. Patent 6,693,321.

Referring to **claims 1 and 4**, the '429 reference discloses in Fig. 1 and respective portions of the specification a nonvolatile semiconductor memory cell comprising:

a semiconductor substrate (11);

a stacked-gate structure that includes a tunnel insulation film (14, column 3, lines 19+), a floating gate electrode (15F), an inter-electrode insulation film (22/25) and a control gate electrode (26), which are stacked on the semiconductor substrate; and

gate side-wall insulation films (28) formed on both side surfaces of the stacked-gate structure,

wherein the thickness of the gate side-wall insulation film increases, at a side portion of the floating gate electrode, from the inter-electrode insulation film (22/25) side toward the tunnel insulation film (14) side, and the width of the floating gate electrode in a channel length direction decreases from the inter-electrode insulation film side toward the tunnel insulation film side.

However, the reference fails to teach that the inter-electrode insulation film (22/25) has a three-layer structure that includes a first oxidant barrier layer, an intermediate insulation layer and a second oxidant barrier layer.

The reference thus fails to teach that the first and second oxidant barrier layers are formed of one of a silicon nitride film and a silicon oxynitride film as claimed in **claim 4**.

Zheng, in also disclosing a nonvolatile semiconductor memory cell comprising a stacked tunnel oxide layer/floating gate layer/inter-electrode insulation film/control gate layer, wherein the inter-electrode insulation film 24 (Fig. 2) comprises a three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30, teaches that the use of a high-k materials, such as silicon nitride, silicon oxynitride, or a refractory metal nitride (paragraph bridging columns 7 and 8) for the three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30 (column 7, lines 19-35) in place of the traditional inter-electrode insulation film helps with, among other advantages, device scaling, high degree of quality, and increased lifetime (column 4, lines 10-34).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '429 reference's inter-electrode insulation film such that it has a three-layer structure. One would have been motivated to make such a change because Zheng teaches that such a structure leads to device scaling, high degree of quality, and increased lifetime. Such a modified device is hereinafter referred to as the '429/321 device and such a teachings the **'429/321 teaching**. Referring to claim 4, Zheng, as cited above, discloses that the first, intermediate, and second layers are formed of one of silicon nitride, silicon oxynitride, and a refractory metal nitride; and because the materials for the first and second layers are the same as claimed, the layers could be called a first oxidant barrier layer and a second oxidant barrier layer as recited in claim 1. As for the intermediate layer, intermediate layer 28 is obviously an intermediate insulation layer.

Referring to **claim 20**, the '429/321 teachings discloses a memory cell as claimed and as detailed above for claims 1 and 4, but fails to teach that the memory cell could be used in a memory chip, which is controlled by a controller. The teachings thus further fails to disclose that the memory chip and the controller are mounted on a single wiring board. However, for the limitation that the memory cell could be used in a memory chip and that which is controlled by a controller, since the teaching does not exclude such usage, such a usage would be obvious to one of ordinary skill in the art at the time the invention was made. As for the limitation that the memory chip and the controller are mounted on a single wiring board, mounting a memory chip and a controller on a single wiring board was what one of ordinary skill in the art would do at the time the invention was made; see, for example, Sato et al. U.S. Patent Application Publication 20020149974, paragraph [0103].

Referring to **claim 5**, the '429 reference further discloses that the gate side-wall insulation films (28) comprises a first side-wall insulation film (28) that is provided on a side surface of the floating gate electrode (15F), and a second side-wall insulation film (28) that is provided on a side surface of the control gate electrode (26).

Referring to **claim 10**, although not shown, a device isolation insulation film is buried at a side surface of the floating gate electrode in a channel width direction for the device to function. See, for example, Takada at el. U.S. Patent 6,649,965, Fig, 2K, which depicts a device isolation insulation film (7) buried at a side surface of a floating gate electrode (8/3) in a channel width direction for the device to function.

7. **Claims 1, 3-5, 10, and 20** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yang U.S. Patent 6,153,904 (the '904 reference) in view of Zheng et al. U.S. Patent 6,693,321.

Referring to **claims 1 and 4**, the '904 reference discloses in Figures 3's, particularly Fig. 3F, and respective portions of the specification a nonvolatile semiconductor memory cell comprising:

a semiconductor substrate (10);

a stacked-gate structure that includes a tunnel insulation film (62, column 3, line 42), a floating gate electrode (68), an inter-electrode insulation film (70) and a control gate electrode (72), which are stacked on the semiconductor substrate; and

gate side-wall insulation films (58/99) formed on both side surfaces of the stacked-gate structure,

wherein the thickness of the gate side-wall insulation film (58/99) increases, at a side portion of the floating gate electrode, from the inter-electrode insulation film (70) side toward the tunnel insulation film side, and the width of the floating gate electrode in a channel length direction decreases from the inter-electrode insulation film side toward the tunnel insulation film side.

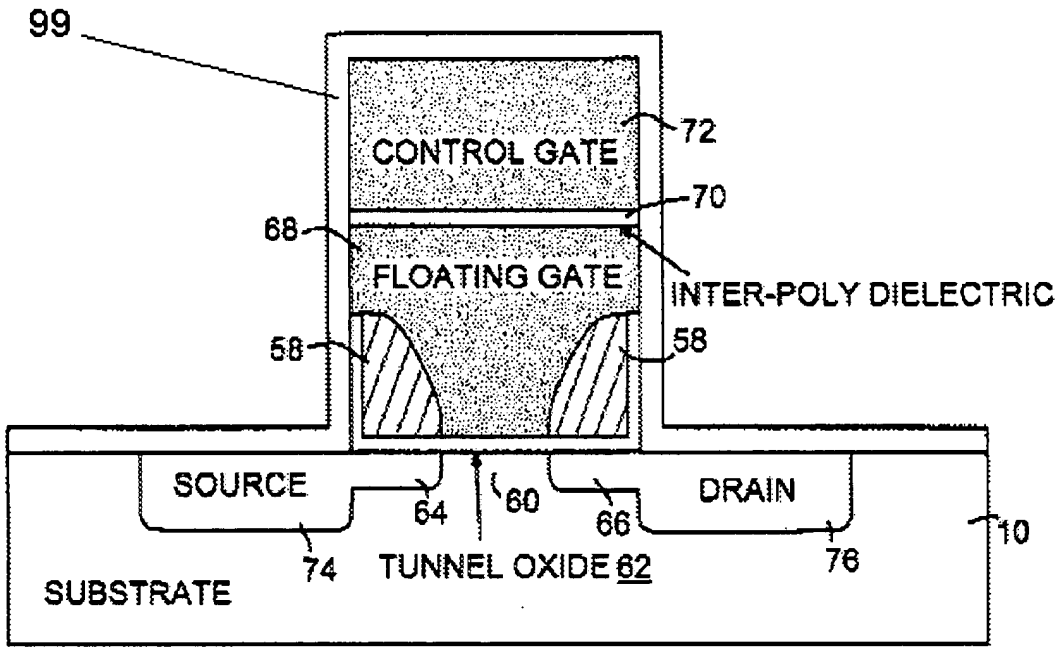

FIG. 3F

Note: 99 is added by the examiner for ease of explanation.

However, the reference fails to teach that the inter-electrode insulation film (70) has a three-layer structure that includes a first oxidant barrier layer, an intermediate insulation layer and a second oxidant barrier layer.

The reference thus fails to teach that the first and second oxidant barrier layers are formed of one of a silicon nitride film and a silicon oxynitride film as claimed in **claim 4**.

Zheng, in also disclosing a nonvolatile semiconductor memory cell comprising a stacked tunnel oxide layer/floating gate layer/inter-electrode insulation film/control gate layer, wherein the inter-electrode insulation film 24 (Fig. 2) comprises a three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30, teaches that the use of a high-k materials, such as silicon nitride, silicon oxynitride, or a refractory metal nitride (paragraph bridging columns 7 and 8) for the three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30 (column 7, lines 19-35) in place of the traditional inter-electrode insulation film helps with, among other advantages, device scaling, high degree of quality, and increased lifetime (column 4, lines 10-34).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '904 reference's inter-electrode insulation film such that it has a three-layer structure. One would have been motivated to make such a change because Zheng teaches that such a structure leads to device scaling, high degree of quality, and increased lifetime. Such a modified device is hereinafter referred to as the '904/321 device and such a teachings the **'904/321 teaching**. Referring to claim 4, Zheng, as cited above, discloses that the first, intermediate, and second layers are formed of one of silicon nitride, silicon oxynitride, and a refractory metal nitride; and because the materials for the first and second layers are the same as claimed, the layers could be called a first oxidant barrier layer and a second oxidant barrier layer as recited in claim 1. As for the intermediate layer, intermediate layer 28 is obviously an intermediate insulation layer.

Referring to **claim 11 and 2**, the '904/321 teachings discloses a memory cell as claimed and as detailed above for claims 1 and 4, but fails to disclose exactly that the width of the

floating gate electrode in the channel length direction is 50 nm or less on a surface of the tunnel insulation film. However, the '904 reference teaches that a width of the floating gate electrode in the channel length direction is 10 nm to 5000 nm on a surface of the tunnel insulation film (Figs. 3A-3C, column 3, lines 32-40, "memory channel region 60, defined by this etching, has a width in the range from 0.01 μm to 5 μm, and is always smaller than the width of central region 52"), which range of width form 10 nm to 5000 nm appears to encompass the claimed range of 50 nm or less. In reference to claim 2, although the '904 reference does not teach that a maximum width of the stacked gate including the gate sidewall spacers (58) is 1.3 or more times as great as the width of floating gate electrode made smaller by the sidewalls (the width of floating gate electrode in the channel length direction on a surface of the tunnel insulation film), as noted above, the reference teaches that the width of the channel region 60 (the same as the claimed "the width of floating gate electrode in the channel length direction on a surface of the tunnel insulation film") is always smaller than the width of central region 52 (the same as the claimed limitation "and a distance between an end portion of one of the gate side-wall insulation films, which end portion is located on a side opposed to the floating gate electrode, and an end portion of the other gate side-wall insulation film, which end portion is located on a side opposed the floating gate electrode", as the width of this central region 52 defines the width of the stacked gate including the gate sidewall spacers (58)), or in other words, the width of the central region 52 is always larger than the width of the channel region 60; and as it appears in Fig. 3F, or as it would be within the ability of a person of ordinary skill in the art, therefore would have been obvious since it requires only routine skills, to form the device with various widths of the regions 52 and 60 such that a maximum width of the stacked gate including the gate sidewall spacers (58) is 1.3 or more times as great as the width of floating gate electrode made smaller by the sidewalls, or in other words, such that a distance between an end portion of one of the gate side-wall insulation films, which end portion is located on a side

opposed to the floating gate electrode, and an end portion of the other gate side-wall insulation film, which end portion is located on a side opposed the floating gate electrode, is 1.3 or more times as great as the width of floating gate electrode in the channel length direction as claimed.

Referring to **claim 20**, the '904/321 teachings discloses a memory cell as claimed and as detailed above for claims 1 and 4, but fails to teach that the memory cell could be used in a memory chip, which is controlled by a controller. The teachings thus further fails to disclose that the memory chip and the controller are mounted on a single wiring board. However, for the limitation that the memory cell could be used in a memory chip and that which is controlled by a controller, since the teaching does not exclude such usage, such a usage would be obvious to one of ordinary skill in the art at the time the invention was made. As for the limitation that the memory chip and the controller are mounted on a single wiring board, mounting a memory chip and a controller on a single wiring board was what one of ordinary skill in the art would do at the time the invention was made; see, for example, Sato et al. U.S. Patent Application Publication 20020149974, paragraph [0103].

Referring to **claim 5**, the '904 reference further discloses that the gate side-wall insulation films (58/99) comprises a first side-wall insulation film (58) that is provided on a side surface of the floating gate electrode (68), and a second side-wall insulation film (99) that is provided on a side surface of the control gate electrode (72).

Referring to **claim 3**, as is evident for Fig. 3F, the inter-electrode insulation film (70) has a substantially flat structure, and an area of the tunnel insulation film, which contacts the floating gate electrode (68), is about 70% or less of an area of the inter-electrode insulation film, which contacts the floating gate electrode.

Referring to **claim 10**, although not shown, a device isolation insulation film is buried at a side surface of the floating gate electrode in a channel width direction for the device to function. See, for example, Takada at el. U.S. Patent 6,649,965, Fig, 2K, which depicts a device isolation insulation film (7) buried at a side surface of a floating gate electrode (8/3) in a channel width direction for the device to function.

8. **Claims 6-8** are rejected under 35 U.S.C. §103(a) as being unpatentable over Yang U.S. Patent 6,153,904 (the '904 reference) in view of Zheng et al. U.S. Patent 6,693,321 and further in view of Kim et al. U.S. Patent Application Publication 20040033653.

Referring to **claims 6-7**, the '904/321 teachings discloses a memory cell as claimed and as detailed above for claims 1, 4, and 5, but fails to teach that the control gate electrode (72, the '904 reference) has a two-layer structure that comprises a high-resistance polysilicon lower layer and a low-resistance silicide upper layer.

Kim, in also disclosing a nonvolatile semiconductor memory cell comprising, for example, a stacked tunnel oxide layer/floating gate layer/inter-electrode insulation film/control gate layer 102/104a/106/108a/110a in Fig. 2, teaches that the control gate electrode having a two-layer structure that comprises a high-resistance polysilicon lower layer (108a) and a low-resistance silicide upper layer (110a) stacked on the polysilicon layer to reduce resistance (paragraph [0009]).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's control gate electrode 72 such that it has a two-layer structure that comprises a high-resistance polysilicon lower layer and a low-resistance silicide upper layer. One would have been motivated to make such a change because Kim teaches that a

control gate electrode having a two-layer structure that comprises a high-resistance polysilicon lower layer and a low-resistance silicide upper layer reduces resistance.

Referring to **claim 8**, Fig. 2 (Kim) shows that an area where an upper surface of the control gate electrode lower layer (108a) contacts a lower surface of the control gate electrode upper layer is substantially equal to an area where a lower surface of the control gate electrode lower layer contacts the inter-electrode insulation film (106).

9. **Claim 9** is rejected under 35 U.S.C. §103(a) as being unpatentable over Yang U.S. Patent 6,153,904 (the '904 reference) in view of Zheng et al. U.S. Patent 6,693,321, further in view of Kim et al. U.S. Patent Application Publication 20040033653, and further in view of Bicksler et al. U.S. Patent Application Publication 20030143814.

Looking at Fig. 3F of the '904 reference, modified in view of Zheng and Kim as noted above to have the three-layer inter-gate insulation film of claim 1 and the two-layer control gate electrode of claim 6, at a stage before formation of a second side-wall insulation film marked as 99 by the examiner (see above). In other words, at this stage, the combined teachings disclose all limitations except for the second side-wall insulation film as recited in claim 9, which second side-wall insulation film is thin at upper and lower surfaces of the control gate electrode lower layer, and thick at a central part of the control gate electrode lower layer. The '904 reference further discloses the required source region 74 and drain region 76.

Bicksler, in also disclosing a nonvolatile semiconductor memory cell, in Fig. 3, comprising a stacked tunnel oxide layer/floating gate layer/inter-electrode insulation film/control gate layer 16/18/20/22/24 over a semiconductor substrate 12 including a source region 26 and a drain region 26, teaches that substrate is ultimately oxidized to repair source/drain damage from the diffusion or other implant of impurities therein, and also to form a

side-wall insulation film in the process (paragraph [0006]). In the same paragraph, Bicksler further teaches that same process will form a second side-wall insulation film (such as 32, Fig. 3) which is thin at upper and lower surfaces of the control gate electrode lower layer (22), and thick at a central part of the control gate electrode lower layer ("silicon dioxide bulges on the sidewalls").

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '904 reference's device, modified in view of Zheng and Kim as noted above to have the three-layer inter-gate insulation film of claim 1 and the two-layer control gate electrode of claim 6, at a stage before formation of a second side-wall insulation film, with the taught step of oxidization. One would have been motivated to make such a change in view of the Bicksler's teachings that that one step of oxidization will repair source/drain damage and also to form a side-wall insulation film, which side-wall insulation film is thin at upper and lower surfaces of the control gate electrode lower layer, and thick at a central part of the control gate electrode lower layer, as claimed.

10. **Claims 1, 4-5, 6-7, and 9** are rejected under 35 U.S.C. §103(a) as being unpatentable over Bicksler et al. U.S. Patent Application Publication 20030143814 (the '814 reference) in view of Zheng et al. U.S. Patent 6,693,321.

The '814 reference discloses in Figs. 1-4 and respective portions of the specification a nonvolatile semiconductor memory cell substantially as claimed.

Referring to **claims 1 and 4**, the '814 reference discloses a nonvolatile semiconductor memory cell comprising:

a semiconductor substrate (12);

a stacked-gate structure that includes a tunnel insulation film (16, "gate dielectric layer", paragraph [0029]), a floating gate electrode (18), an inter-electrode insulation film (20) and a control gate electrode (22), which are stacked on the semiconductor substrate; and

gate side-wall insulation films (34/32) formed on both side surfaces of the stacked-gate structure,

wherein the thickness of the gate side-wall insulation film increases, at a side portion of the floating gate electrode, from the inter-electrode insulation film (20) side toward the tunnel insulation film (16) side, and the width of the floating gate electrode in a channel length direction decreases from the inter-electrode insulation film side toward the tunnel insulation film side (as clearly depicted in Fig. 3).

However, the reference fails to teach that the inter-electrode insulation film (20) has a three-layer structure that includes a first oxidant barrier layer, an intermediate insulation layer and a second oxidant barrier layer.

The reference thus fails to teach that the first and second oxidant barrier layers are formed of one of a silicon nitride film and a silicon oxynitride film as claimed in **claim 4**.

Zheng, in also disclosing a nonvolatile semiconductor memory cell comprising a stacked tunnel oxide layer/floating gate layer/inter-electrode insulation film/control gate layer, wherein the inter-electrode insulation film 24 (Fig. 2) comprises a three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30, teaches that the use of a high-k materials, such as silicon nitride, silicon oxynitride, or a refractory metal nitride (paragraph bridging columns 7 and 8) for the three-layer structure 26/28/30 including first layer 26, intermediate layer 28, and second layer 30 (column 7, lines 19-35) in place of the traditional

inter-electrode insulation film helps with, among other advantages, device scaling, high degree of quality, and increased lifetime (column 4, lines 10-34).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '814 reference's inter-electrode insulation film such that it has a three-layer structure of high-k materials. One would have been motivated to make such a change because Zheng teaches that such a structure leads to device scaling, high degree of quality, and increased lifetime. Such a modified device is hereinafter referred to as the '814/321 device and such a teachings the **'814/321 teaching**. Referring to claim 4, Zheng, as cited above, discloses that the first, intermediate, and second layers are formed of one of silicon nitride, silicon oxynitride, and a refractory metal nitride; and because the materials for the first and second layers are the same as claimed, the layers could be called a first oxidant barrier layer and a second oxidant barrier layer as recited in claim 1. As for the intermediate layer, intermediate layer 28 is obviously an intermediate insulation layer.

Referring to **claim 5**, the '814 reference further discloses that the gate side-wall insulation films (34/32) comprises a first side-wall insulation film (34) that is provided on a side surface of the floating gate electrode (18), and a second side-wall insulation film (32) that is provided on a side surface of the control gate electrode (22).

Referring to **claims 6-7**, the '814 reference further discloses that the control gate electrode (22/24) (optionally) has a two-layer structure that comprises a high-resistance polysilicon lower layer (22) and a low-resistance silicide upper layer (24, paragraphs [0029], polysilicon lower layer 22 and WSi upper layer 24).

Referring to claim 9, the '814 reference further discloses that the second side-wall insulation film (32) is thin at upper and lower surfaces of the control gate electrode lower layer (22), and thick at a central part of the control gate electrode lower layer (Fig. 3 and paragraph [0006]: "bulges").

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
June 16, 2005